of the NMOS transistor **200** is coupled to the drain **170** of the PMOS transistor **210**. Thus the total current flow from the node comprising the n-drain **125** and the p-source **135**, to the node comprising the n-source **145** and the p-drain **170**, is $I_{ds\text{-}n}+I_{sd\text{-}p}$, i.e., the sum of the drain-to-source current $I_{ds\text{-}n}$ of the NMOS device **200** and the source-to-drain current $I_{sd\text{-}p}$ of the PMOS device **210**.

FIG. **3** is graph representing drain-to-source current I_{ds} and drain-to-source resistance R_{ds} as a function of drain-to-source voltage V_{ds} at maximum gate biases for a dual-gate, bimodal conduction LDMOS such as that shown in FIG. **1**. Plot **300** represents the on-state drain-to-source current $I_{ds\text{-}n}$ when the dual-gate, bimodal conduction LDMOS **100** when the device is operated as an NMOS device, i.e., when the voltage at the n-gate **180** causes the n-channel **105** to conduct while the voltage at the p-gate **185** causes the p-channel **120** to be turned off. Plot **310** represents the associated on-state drain-to-source resistance $R_{ds\text{-}n}$ when the LDMOS integrated circuit **100** is operated as an NMOS device. Plot **320** represents the on-state drain-to-source current $I_{ds\text{-}pn}$ when the dual-gate, bimodal conduction LDMOS **100** when the device is operated as a bimodal conduction p-n device, i.e., when the voltage at the n-gate **180** causes the n-channel **105** to conduct while the voltage at the p-gate **185** simultaneously causes the p-channel **120** to conduct. Note that when referring to the drain-to-source current $I_{ds\text{-}pn}$ of the p-n bimodal LDMOS **100**, this refers to the current flowing from the drain **125** of the NMOS transistor **200** (which is coupled to the source of the PMOS transistor **210**) to the source **145** of the NMOS transistor **200** (which is coupled to the drain **170** of the PMOS transistor **210**). Plot **330** represents the associated on-state drain-to-source resistance $R_{ds\text{-}pn}$ when the LDMOS integrated circuit **100** is operated as a bimodal conduction p-n device. As can be seen in FIG. **3**, I_{ds} for both the unimodal NMOS conduction mode **300** and the bimodal p-n conduction mode **320** increases in a substantially linear fashion until the device saturates (between 20V and 40V for the illustrative device represented by FIG. **3**). Similarly, the on-resistance R_{ds} for both the unimodal NMOS conduction mode **310** and the bimodal p-n conduction mode **330** increases quite linearly until the device saturates. As can be seen in FIG. **3**, operating the LDMOS device **100** as a bimodal p-n device significantly enhances I_{ds}, and therefore reduces R_{ds}, in both the linear region and the saturation region.

Specific on-resistance R_{sp} for a power device is usually measured at very low V_{ds}, where the device operates in the linear region. However, the maximum output current in power switching circuits is determined by the saturation drain-to-source current $I_{ds,sat}$, defined at the saturation voltage $V_{ds,sat}$, and the thermal dissipation. Also, the on-state current and corresponding drain-to-source voltage V_{ds} for a power switch varies with different load conditions. Therefore, it is desirable to have a smaller slope for the linear plot of R_{ds} vs. V_{ds} when the switch is on. As can be seen in FIG. **3**, the p-n bimodal conduction enhances the drive current by at least 30% at V_{ds} of 20V compared to n-type conduction only. With the slave p-gate **185** fully on, the $R_{ds\text{-}pn}$ **330** dependence on V_{ds} before the device saturates is minimized with a slope of 2.5% increase per volt, which can lead to lower conduction loss and lower thermal dissipation. In contrast, the $R_{ds\text{-}n}$ **310** of n-conduction LDMOS increases with V_{ds} at a rate of approximately 5% per volt.

FIG. **4** is a cross-sectional view of a RESURF-based dual-gate LDMOS integrated circuit **400** with p-n bimodal conduction. The LDMOS integrated circuit **400** comprises a p-type LDMOS transistor having an n-type transistor embedded therein. In that sense, the LDMOS device **400** is the inverse of the LDMOS device **100** of FIG. **1**, which comprises an n-type LDMOS transistor having a p-type transistor embedded therein. The p-type transistor of the LDMOS integrated circuit **400** will at times be referred to herein as a PMOS device. Similarly, the n-type transistor of the LDMOS integrated circuit **100** will at times be referred to herein as an NMOS device. The LDMOS integrated circuit **400** includes a p-type region **405** formed over an n-type substrate **410**, and an n-type RESURF layer **415** buried within the p-type region **405**. An n-type top layer **420** of the LDMOS device **400** is formed on top of the p-type region **405** and serves as a RESURF region. As mentioned, the n-type buried layer **415** and the n-type top layer **420** function as RESURF regions, which means they serve to reduce an electric field in their respective adjacent p-type regions **405**.

A drain electrode **425** is coupled to a highly positively doped (p+) implant **440** that is embedded in the p-type region **405**. The drain electrode **425** serves as the drain of the p-type LDMOS transistor of the integrated circuit **400**. The drain electrode **425** of the p-type transistor is also electrically coupled to a second electrical contact **435** that is coupled to an n+ implant **430**, or region, that is embedded in the p-type region **405**. The second contact **435** serves as the source of the NMOS transistor that is embedded in the integrated circuit **400**. The source of the NMOS transistor will at times be referred to herein as the n-source **435**.

A source electrode **445** is coupled to a p+ implant **460** that is embedded in an n-type well **165** within the n-type region **405**. The source electrode **445** serves as the source of the p-type LDMOS transistor of the integrated circuit **400**. The source electrode **445** of the n-type transistor is also electrically coupled to a second electrical contact **470** that is coupled to an n+ implant **475** that is embedded in the top n-type layer **420**. The second contact **470** forms the drain of the NMOS transistor that is embedded in the integrated circuit **400**. The n-type top RESURF region **420** thus serves as a drain extension of the NMOS. The second contact **470** constituting the drain of the n-type transistor will at times be referred to herein as the n-drain. In an illustrative embodiment, the source electrode **445** of the p-type transistor is also electrically coupled to a third electrical contact **455** that is coupled to a highly negatively doped (n+) implant **450** that is embedded in the n-well **465**. The third contact **455** forms part of the drain of the NMOS transistor, together with the drain contact **470** coupled to the top n-type layer **420**. In such an embodiment, the buried n-type RESURF region **415** thus serves as a further drain extension of the NMOS.

The voltage present at the p-gate **485** controls the current flow from the source **445** to the drain **425** of the p-type LDMOS transistor of the integrated circuit **400**. The source-to-drain current $I_{sd\text{-}p}$ of the p-type transistor comprises holes flowing from the source **445** to the drain **425** in the top and bottom channels of the p-type region **405**, as shown in FIG. **4**.

The voltage present at the n-gate **480** controls the current flow from the drain **470** of the n-type transistor to the source **435** of the n-type transistor of the integrated circuit **400**. In an illustrative embodiment, the drain-to-source current $I_{ds\text{-}n}$ of the n-type transistor comprises electrons flowing from the n-source **435** to the n-drain **470** in the top n-type layer **420**, as shown in FIG. **4**.

In an illustrative embodiment, the drain-to-source current $I_{ds\text{-}n}$ further comprises electrons flowing from the n-source **435** to the n-drain **455** in the buried n-type layer **415**. In an illustrative embodiment, the integrated circuit **400** includes,